

AMENDMENTS TO THE DRAWINGS:

The replacement sheet in the Appendix includes a new Figure 2. The new Figure 2 provides a better rendition of the subject matter depicted therein.

REMARKS

The specification and drawings have been amended to make editorial changes therein, bearing in mind the criticisms in the Official Action, to place the application in condition for allowance at the time of the next Official Action.

Art was not applied against claims 20-28 and it is presumed that this is an indication that these claims include patentable subject matter<sup>1</sup>. In reliance thereon, these claims have been amended as to form. Allowance of claims 20-28 is respectfully requested.

Claims 2-29 and 31-32 were rejected under §112, second paragraph, and have been amended as to form. It appears that the Official Action may not have considered the Preliminary Amendment filed with the application on December 30, 2004. Please note that claims 21 and 31 in the Preliminary Amendment do not include "the step" recited in paragraph 10 of the Official Action. Support for the amendment to claim 24 is found in Table 1 at page 42. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 1, 15, 29, and 31-32 were rejected as anticipated by YOSHIDA 6,303,405. Claim 1 and 15 have been canceled and claims 29 and 31-32 have been amended to depend from

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<sup>1</sup> Paragraph 11 of the Official Action acknowledges that the subject matter of claims 20-23 is not found in YOSHIDA, but subsequent paragraphs do not indicate where the missing features are to be found in the other references. There is no mention of claims 24-28.

claim 2. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 2-19 were rejected as unpatentable over YOSHIDA in view of MIKI et al. 6,800,501 and KUSUMOTO et al. 4,849,260. Reconsideration and withdrawal of the rejection are respectfully requested.

YOSHIDA et al. teach in Figures 1A-1D and Figure 2-3, a process for producing a group III nitride semiconductor substrate that includes the steps of:

forming a GaN layer 12, AlGaN layer 13 and n-type GaN layer on a sapphire substrate 11 by MOCVD method, wherein as the Al composition in the AlGaN layer is approximately 30% and it is formed thick, cracks 20A are produced over the entire surface of the AlGaN layer, and thus the AlGaN layer 13 having said defective parts (i.e., cracks 20A) is susceptible to a stress and function as a "lift-off layer" for separating the substrate,

forming an n-type GaN layer 15 up to a thickness around 80  $\mu\text{m}$ , and followed by formation of a multi-layered structure 16, and

separating the substrate 11 by applying a stress through fitting a tool onto a side surface or bottom surface of the substrate 11 and frictionally moving the tool so that separation occurs near the front and back interface of the AlGaN layer 13 as the "lift-off layer" susceptible to said stress applied. (see column 5, line 63 to column 7, line 36).

YOSHIDA et al. explain the mechanism of separation of the substrate 11 using the AlGa<sub>N</sub> layer 13 as the "lift-off layer" susceptible to the stress applied. The cracks 20A are densely produced during formation of the AlGa<sub>N</sub> layer 13 due to a lattice distortion derived from Al that is contained as one of group III components for said AlGa<sub>N</sub> alloy semiconductor. In addition, when the wafer is held at the growth temperature just after growth of the AlGa<sub>N</sub> layer 13, parts of the underlying Ga<sub>N</sub> layer 12 under the cracks 20A formed through the AlGa<sub>N</sub> layer 13 are etched by hydrogen contained in the growth atmosphere, and thereby voids 20B are produced at the interface region of the Ga<sub>N</sub> layer 12. On the other hand, when the n-type Ga<sub>N</sub> layer 14 is grown on the AlGa<sub>N</sub> layer 13, portions above the cracks 20A are also buried continuously and flat with the n-type Ga<sub>N</sub> layer 14 because of two-dimensional growth occurring at the stage of growth of the n-type Ga<sub>N</sub> layer 14. Accordingly, no adverse affection is given to the n-type Ga<sub>N</sub> layer 15 grown on the n-type Ga<sub>N</sub> layer 14. (see column 6, lines 47-65, and Figure 2).

The cracks 20A produced in the AlGa<sub>N</sub> 13 and the voids 20B formed at the parts of the Ga<sub>N</sub> layer 12 under the cracks 20A physically weaken the interfaces with the AlGa<sub>N</sub> layer 13 as the "lift-off layer". Therefore, when a stress is applied to the interfaces with the AlGa<sub>N</sub> layer 13 as mentioned above, the separation starts from the cracks 20 and the voids 20B. In the result, separation occurs near the front and back interface of

the AlGa<sub>N</sub> layer 13 as the "lift-off layer" susceptible to the stress applied mechanically by using the tool (see column 6, line 66 to column 7, line 3).

In place of the AlGa<sub>N</sub> layer 13, the InGa<sub>N</sub> layer 21 is employed as the "lift-off layer", as shown in Figure 3. That is, the InGa<sub>N</sub> layer 21 is provided between the Ga<sub>N</sub> layer 12 and the n-type Ga<sub>N</sub> layer 14. Pits 20 that are caused presumably by phase separation of In are produced in a high density during growth of said InGa<sub>N</sub> layer 21. The pits 20C are fine bores passing through the InGa<sub>N</sub> layer 21, and are distributed as dense as 107 pieces to 109 pieces per cm<sup>2</sup> in most cases. The pits 20C make the InGa<sub>N</sub> layer 21 physically fragile, and thus separation occurs near the front and back interface of the InGa<sub>N</sub> layer 21 as the "lift-off layer" susceptible to a stress applied.

However, when the InGa<sub>N</sub> layer 21 is employed as the "lift-off layer", there is no suggestion that any voids would be produced in the underlying Ga<sub>N</sub> layer 12.

As explained above, YOSHIDA et al. teach nothing more than the voids 20B that are produced through such a mechanism that parts of the underlying Ga<sub>N</sub> layer 12 under the cracks 20A formed through the AlGa<sub>N</sub> layer 13 are etched by hydrogen contained in the growth atmosphere. Of course, the underlying Ga<sub>N</sub> layer 12 is formed prior to the growth of the AlGa<sub>N</sub> layer 13.

However, YOSHIDA et al. teach nothing about such a local structure where a group III nitride semiconductor layer

including region of voids therein is formed on the metal element-containing film, and the formation of voids are caused by the decomposing action of the metal element contained in the metal element-containing film.

MIKI et al. teach the light-permeable electrode comprising a very thin metal film that are formed by such a process in which the metal film is first formed by vapor deposited and then the metal film is heat-treated at a temperature of 500°C or higher to induce sublimation of the metal, so that the resulted thickness is reduced to from 0.001 to 1  $\mu\text{m}$  to thereby impart light permeability. Further, MIKI et al. teach such a metal as Au, Ni, Pt, In, Cr or Ti is suitably used as the electrode material, which can be sublimated by heat treatment to reduce the thickness thereof. (see column 1, line 64 to column 2, line 8).

However, MIKI et al. fail to teach anything as to metal element having a decomposing action on a group III nitride semiconductor, which decomposing action is used to form voids within a layer made of said group III nitride semiconductor that is grown on the metal element-containing film.

KUSUMOTO et al. teach such a structure formed by a process comprising steps of:

forming an insulating film 60 of  $\text{SiO}_2$  on a substrate 55a of the wafer 55, as shown in Figure 2,

forming via holes (or contact holes) 60a in the insulating film 60, and

forming a metallic film 58 rapidly on the substrate 55a in the via holes 60a, as shown in Figure 3.

Accordingly, the surface of the wafer 55a is covered with the insulating film 60 of  $\text{SiO}_2$  with the via holes 60a and the metallic film 58 formed in the via holes 60a. The metallic film 58 formed in the via holes 60a blocks direct contact between the second metallic films 59 and the surface of the wafer 55.

If the metallic film 58 formed in the via holes 60a is completely removed away, the resulted film that is consisted only of the insulating film 60 of  $\text{SiO}_2$  with the via holes 60a is by no means a metal element-containing film.

In view of these facts pointed out, combination of YOSHIDA et al. with MIKI et al. or with KUSUMOTO et al. can never lead to the invention of the present application, as all of the three references fail to teach or suggest at least said local structure where a group III nitride semiconductor layer including region of voids therein is formed on the metal element-containing film, and the formation of voids are caused by the decomposing action of the metal element contained in the metal element-containing film.

Accordingly, these claims avoid the rejection under §103.

Claims 1-5 and 15-19 were also rejected on the ground of nonstatutory obviousness-type double patenting over claims 1-5 and 36 of US Patent 6,924,159.

The claimed invention of U.S. 6,924,159 is a process for manufacturing a semiconductor substrate made of a group III nitride comprising the steps of:

forming a metal film on a basal substrate having a first semiconductor layer of a group III nitride formed on a base material or basal substrate comprising a first semiconductor layer of a group III nitride,

heat-treating said basal substrate in an atmosphere containing hydrogen gas or hydrogen-containing compound gas to form voids in said first semiconductor layer of the group III nitride, and

forming a second semiconductor layer of a group III nitride on said metal film.

As explained above, the claimed process of U.S. 6,924,159 has no definition about such a step of forming voids in the second semiconductor layer of the group III nitride formed on the metal film, which step should be conducted at least post to the step of heat-treating said basal substrate in an atmosphere containing hydrogen gas or hydrogen-containing compound gas to form voids in said first semiconductor layer of the group III nitride. However, the step of heat-treating to form voids in said first semiconductor layer of the group III nitride that is



underlying under the metal film is essential to the claimed process of U.S. 6,924,159.

On the other hand, in the claimed process of the present application, the step of forming a group III nitride semiconductor layer including region of voids therein on the metal element-containing film to be brought into direct contact therewith is an essential step. However, such a step of heat-treating to form voids in the semiconductor layer of the group III nitride that is underlying under the metal film is by no means essential to the claimed process of the present application.

In view of these distinctions between the present application and U.S. 6,924,159, the claimed invention of the present application is not obvious from the claimed invention of U.S. 6,924,159.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

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On the other hand, in the claimed process of the present application, the step of forming a group III nitride semiconductor layer including region of voids therein on the metal element-containing film to be brought into direct contact therewith is an essential step. However, such a step of heat-treating to form voids in the semiconductor layer of the group III nitride that is underlying under the metal film is by no means essential to the claimed process of the present application.

In view of these distinctions between the present application and U.S. 6,924,159, the claimed invention of the present application is not obvious from the claimed invention of U.S. 6,924,159.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

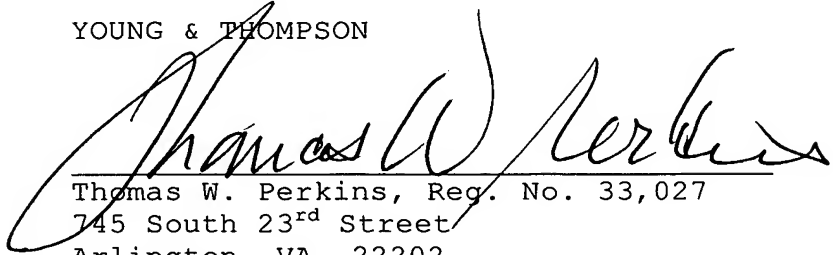
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Respectfully submitted,

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A large, stylized handwritten signature in black ink, appearing to read "Thomas W. Perkins", is written over the printed name and address.

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